Single Device Characterization by Nano-probing to Identify Failure Root Cause

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Abstract

In general failure analysis cases, a less invasive fault isolation approach can be utilized to resolve a visual root cause defect. In the case of nano technology, visual defects are not readily resolved, due to an increase in non-visible defects. The non-visible defects result in a lower success rate since conventional FA methods/tools are not efficient in identifying the failure root cause. For the advanced nanometer process, this phenomenon is becoming more common; therefore the utilization of advanced techniques are required to get more evidence to resolve the failure mechanism. The use of nanoprobe technology enables advanced device characterization in order to obtain more clues to the possible failure mechanism before utilizing the traditional physical failure analysis techniques.

Introduction

With the continued growth of the IC (Integrated Circuit) industry, (technology driving down to 90nm and below), inspection and deprocessing tools have been developed that are able to keep up with the advancing and demanding imaging requirements [1]. However, the fault isolation techniques for nanometer devices have not been able to keep up with the technology and failure analysis on these nodes are become more challenging.

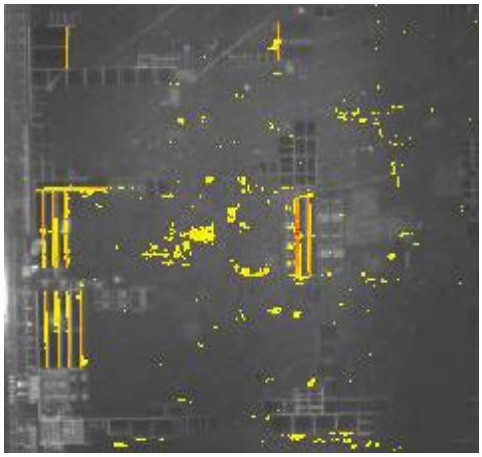
In earlier processes, WAT (Wafer Acceptance Test) parameters were good enough to monitor the behavior of devices in chips; however for more complicated and shrinking ULSI technology, this approach can't accurately reflect the behavior of all devices contained within the chip. A traditional device measurement technique was to utilize a FIB to deposit metal pads and then probe the pads using tungsten needles on a micro-probe station. This methodology requires large metal spacing and suffers from noise during device measurements, and is becoming more difficult due to the shrinking technology. Nano-probing is an alternative method that will overcome this predicament. Nano-probing is capable of directly measuring the behavior of source/drain junctions with a single probe, resistance measurement of two contacts with two probes, and full transistor characterization with multiple probes.

With the obvious advantages of nano-probing, it is important to note several disadvantages, such as contact resistance, tip oxidation, sample preparation, and test-timing issues affect the accuracy of probing result [2]. In order to achieve low Rc on nanometer features, probe tips and the sample surface must keep clean and free of oxides [3]. Excluding the issues noted above, the probing results are reliable for electrical characterization analysis.

Basic transistor parameters such as V_t, I_{off}, I_{sat}, and junction behavior can be identified by means of I/V curves measurements. This capability will help guide the root cause failure analysis when comparing the measured data with reference data.

PFA procedure

In this article, an embedded SRAM of an 110nm product was malfunctioning. Our first approach was to perform emission microscopy in an effort to isolate the potential failure area. The abnormal emission spots that are different with reference are showing in Figure 1. After mapping the emission spots to the layout, a PMOS transistor was identified as an area to focus the PFA techniques. A top down analysis utilizing parallel lapping and PVC techniques down to the contact level failed to reveal any obvious abnormalities. Since no visible defects were observed, additional characterization is needed to better understand the cause of the emitting PMOS transistor.



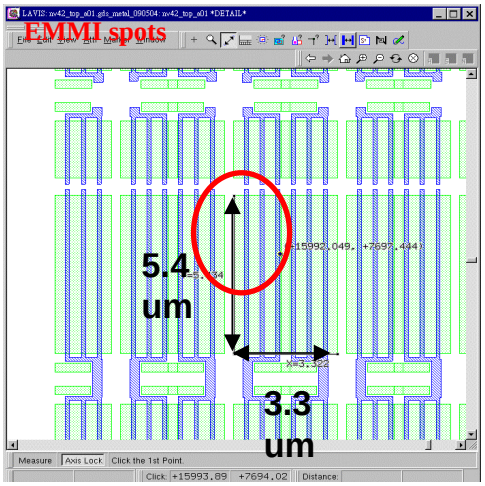
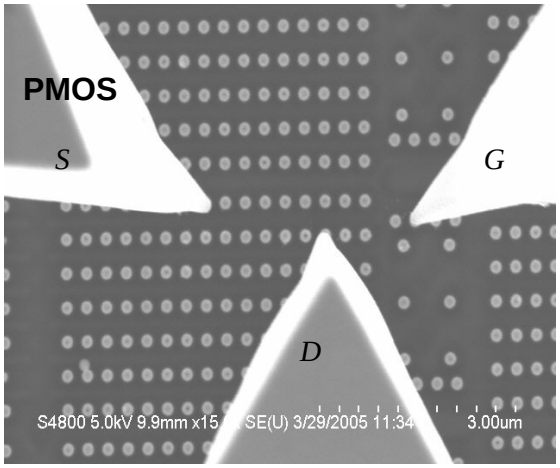


Figure 1. Using EMMI to isolate abnormal positions. Layout shows the EMMI spots locate on PMOS area.

Device Characterization

A wafer probing system with three micromanipulators (Klocke Nanotechnik) was used in the measurements, which was installed into a Hitachi FE-SEM S-4800. Utilizing this nano-probing technique, we can measure the device characteristics at the contact level (Figure 2). After comparing the I/V curves of the emitting PMOS transistor with a reference PMOS transistor, an abnormal electrical characteristic can be observed on the emitting transistor (See Figure 2). The I/V curve of bad transistor shows a lower I_{sat} and higher I_{off} current. In order to understand the leakage path, the current components of Source, Drain, Gate, and Well/substrate node shall be checked (See Table 1). Analysis of the electrical results indicates the leakage path of the emitting transistor is between drain and substrate.

In order to further validate the electrical measurements, a PMOS transistor on the periphery was also used for confirmation. After comparing its result with a reference, the behavior was the same. So the difference of PMOS found is reliable, it should be something abnormal to cause drain to substrate leak.



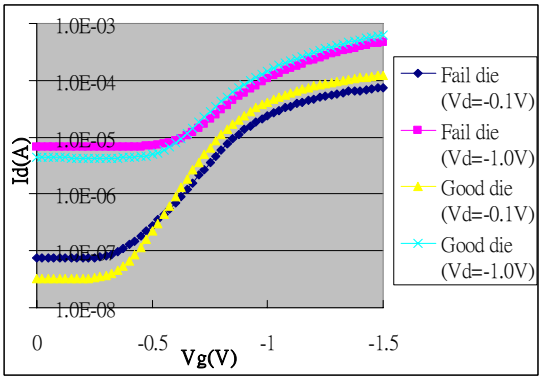


Figure 2 Device behavior is different between the PMOS transistors of bad and good dice. The device of bad die has higher Ioff.

Current flow		Id (uA)	Ig (uA)	Is (uA)	Ib (uA)
Bad die	Ioff	**-6.81**	6.08E-5	**1.83**	**4.99**
	Isat	-113.66	-0.00523	106.45	**7.06**
Good die	Ioff	-1.27	2.04E-5	1.11	0.164
	Isat	-155.04	-0.00734	155.07	0.197

Table1. It shows the current value of source, drain, gate, and well/substrate. Strong signals labeled with red indicate leakage existed between drain and substrate.

Result

The conductive-AFM (C-AFM) has already been widely used in FA cases and has become a standard FA tool to identify failure location and help for realizing the failure mechanism by current map and I/V curve [4]. As mentioned above, the emitting PMOS transistor was caused by a junction leakage issue. To further confirm the results obtained using nano-probe technique, C-AFM technique was used. A current map of the area was obtained using a CAFM (shown in Figure 3) In the current mapping image (positive bias from substrate to tip), the N+ contact area is chosen to display a bright color; however the P+ contact area shows the same color as the N+ contact. This behavior indicated there was a leakage path between P+ contact and substrate. Checking the I/V curves of the different contacts to substrate (Figure 3), the behavior of P+/N-well (blue curve) seems like that of P-well pick up (yellow curve), not a normal P+/N-well (pink curve). This phenomenon is meaningful, and it indicates the leakage is most likely caused by a well issue.

To prove this theory, PFA evidence for N-well implant was needed. Figure.4 shows the plane view junction stain and x-section SCM (Scanning Capacitance Microscope) images. In plane view junction stain image, there is no difference of contrast between N-well and P-well, so the theory of a missed N-well implant issue seems more probable. In the SCM x-section image, the N type implant signals will be set on bright colors. However, in the N-well implant area, the signals are not clear. This result indicates no N-well implant is indeed

the root cause. After verifying all of the N-well implants steps, the mask issue of N-well implant is identified.

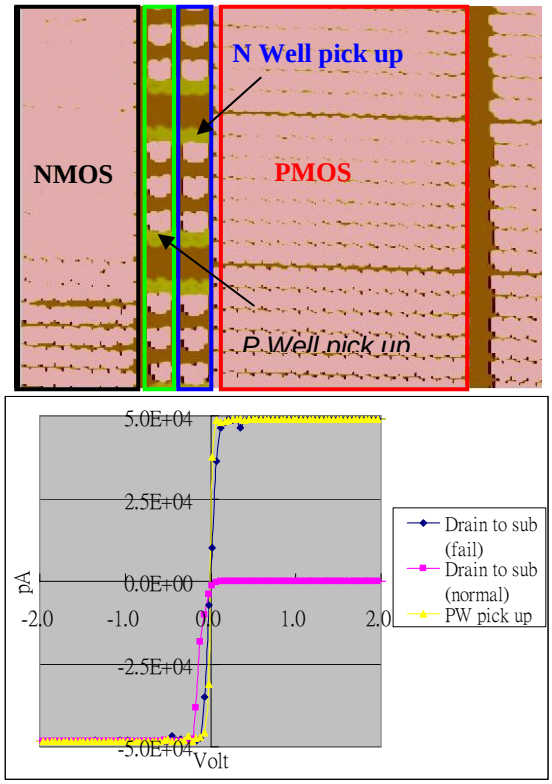


Figure 3 The P-well of current mapping image should be dark. The I/V of abnormal drain to substrate seems like P-well pick up behavior.

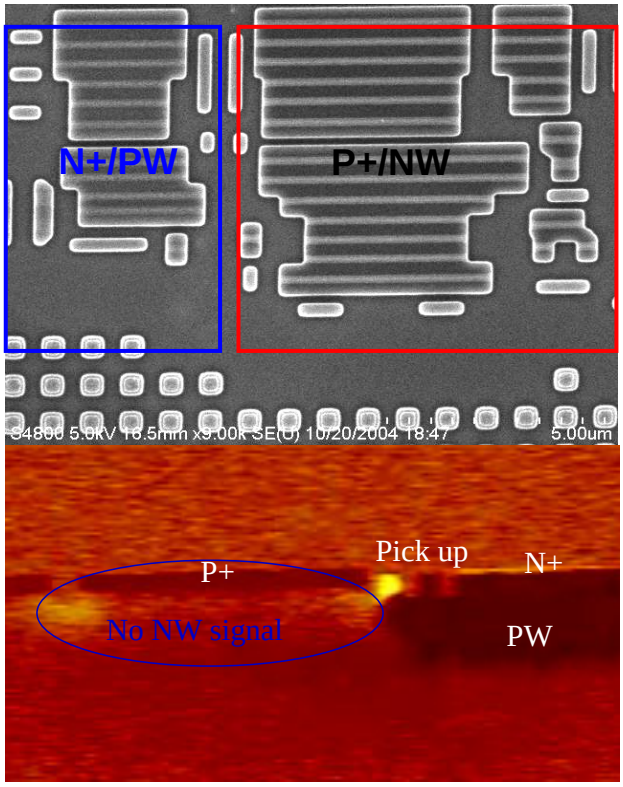


Figure 4. Junction stain shows there is no difference of contrast between N-well and P-well, which should be due to the problem of N-well miss implant. A SCM x-section image indicates no N-well implant indeed.

Conclusion

Generally, nano-probing system is a powerful tool for electrical analysis; it can be used to characterize junction behavior, short/resistance and transistor/diode measurements. For device behavior checking, the basic parameters, such as V_t, I_{off}, and I_{sat} can be measured easily, and the current flow to source, drain, gate, and well/substrate should also be identified to realize the leakage path.

Because WAT parameters can't accurately reflect real device behavior in circuit, the nano-probing measurements on suspected transistors are needed. It can obtain more electrical data to provide more hints, and saving more time to identify the root cause for the FA of 130nm technology and below.

Reference

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